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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,902	03/11/2004	Sam Gat-Shang Chu	AUS920031079US1	7019

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,902	CHU ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 are presented for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 8-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claims 8-10, claimed invention including "a second and third tri-state inverters", which was not described in written description or drawing.

Regarding claims 11-17, claimed invention including "a transmission gate circuit". As described in paragraph 0021 "the tri-state inverter 202 is replaced with transmission gate multiplexor circuit comprising transmission gate 220 and inverter 221". Since 202 in Figure 2 is an inverter only, it is not a multiplexor circuit. With understanding of examiner the function of a mux is different from function of an inverter, and "the multiplexor 205 is replaced by a transmission gate multiplexor circuit comprising transmission gate 330 and inverter 331 in Figure 6". As shown in Figure 5, the design of this embodiment is mux 205 is coupled **from output of bit line**, while the design of

Figure 6 of present invention, transmission gate multiplexor circuit comprising transmission gate 330 and inverter 331 is **input to bit line.** Examiner does not understand how can replacing a mux 205 by transmission 330 and inverter 331, because they are not the same location and do difference function in design. In written description applicant discloses "a transmission gate multiplexor" comprising *transmission gate 330 and inverter 331*. A "transmission gate circuit" is not defined in specification.

Regarding claims 7, 17, the limitation "wherein a multiplexer is not coupled between the bit line and latch" is not a claimed invention, because none of mux is used in claimed invention.

Claims must be canceled.

Regarding claim18, as described above, "transmission gate" is not defined in written description, "transmission gate multiplexor" is defined in written description, which including a transmission gate and an inverter.

As described above, the name of element using in claim should be same name as defined in written description.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1-6, 11-16 are rejected under 35 U.S.C. 102(a) as being clearly anticipated by Applicant Admitted Prior Art (AAPA).

. Regarding claims 1-6, 11-16, Figures 2,5 of AAPA disclose a register file (200) comprising a plurality of register file cells (100) coupled to a bit line (GBL) a latch coupled to the bit line (207), and an inverter (204) coupled between an output (OUT) of the latch (207) and the bit line (GBL), and comprising another inverter (202) coupled between the bit line and an input of the latch, and wherein the output of the latch is an output of the register file (Figures 2,5, OUT), and wherein the inverter is a tri-state inverter (202) receiving a hold select signal (Local Select) to control operation of the inverter, and where the inverter tri-state inverter receiving a hold select signal to control operation of the inverter (Figure 5, 205, 206), and data is read out of the register array to be input into the latch (Figures 2, 5).

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1-7,11-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Chu et al. (Pub. U.S. Patent No. 2005/0099851).

Regarding claims 1-7, Chu et al. disclose a register file (Figure 1A, 100) comprising: a plurality of register file cells (Figure 1E, 124) coupled to a bit line; a latch (Figure 1E, I1,I2) coupled to the bit line; and an inverter (Figure 1C, I0) coupled between an output of the latch and the bit line, and comprising another inverter (Figure 1E, I3) coupled between the bit line and an input of the latch, and wherein the output of the latch is an output of the register file (Figure 1E), and wherein the inverter is a tri-state inverter receiving a hold select signal (Figure 1C, SEL_0) to control operation of the inverter, and wherein an output of the inverter is coupled to the bit line and wherein an input of the inverter is coupled to the output of the latch (Figure 1E, 1C, output from 1E to 1C), and wherein data is read out of the register array to be input into the latch (Figure 1E, WR_DATA), and wherein a multiplexor is not coupled between the bit line and the latch (no multiplexor is coupled between bit line and latch).

Regarding claims 11-17, Chu et al. disclose a register file (Figure 1A) comprising: a plurality of register file cells (Figure 1E, 124) coupled to a bit line, a latch coupled to the bit line (Figure1E, I1, I2); and a transmission gate circuit (Figure 1C, 122) coupled between an output of the latch and the bit, and an inverter (Figure 1E, I3) coupled between the bit line and an input of the latch, and wherein the output of the latch is an output of the register file (Figure 1E), and wherein the transmission gate circuit receives a hold select signal (Figure 1C, 0039), and wherein an output of the transmission gate circuit is coupled to the bit line and wherein an input of the transmission gate circuit is

coupled to the output of the latch, and wherein data is read out of the register array to be input into the latch (Figure 1C, [0039]), and wherein a multiplexor is not coupled between the bit line and the latch (Figures 1, no mux is used).

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-7,11-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Henkels et al. (U.S. Patent No. 5,481,495).

Regarding claims 1-4, 7,11-14,17, Henkels et al. disclose a register file (Figure 1) comprising: a plurality of register file cells coupled to a bit line (Figure 1, BL) ; a latch coupled to the bit line (Figure 1, 11,12); and an inverter (Figure 1, 15) coupled between an output of the latch and the bit (Figure1, inverter 15 located between output of latch B and BIT Line), and further comprising an inverter (Figure 5, 55,56, Column 4, lines 15-19) coupled between the bit line and an input of the latch, and wherein the output of the latch is an output of the register file (Column 4, lines 20-25), and wherein the inverter is a tri-state inverter receiving a hold select signal (Column 4, lines 15-20), and wherein a multiplexor is not coupled between the bit line and the latch (Figure 1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thong Q. Le
Primary Examiner
Art Unit 2827

10/25/2006